What is claimed is:

1. A method of synchronizing with a clock signal comprising:
receiving a first input clock signal having a clock signal time period;
subtracting a first time period from the first input clock signal, where the first time period is a static component;
subtracting a second time period from the first input clock signal, where the second time period is equivalent to a real data path;
measuring a remaining time period of the first input clock signal upon receiving a second input clock signal;
delaying the second input clock signal the first time period to produce a delayed second input clock signal; and
adding the remaining time period of the first input clock signal to the delayed second input clock signal.

2. The method of claim 1, wherein the static component is a static component of the clock signal time period.

3. The method of claim 1, wherein the static component is greater than the clock signal time period.

4. A method of synchronizing with a clock signal comprising:
receiving a first input clock signal having a clock signal time period;
delaying the first input clock signal a first time period, where the first time period is a static component;
delaying the first input clock signal a second time period, where the second time period is equivalent to a real data path;
measuring a remaining time period of the first input clock signal upon receiving a second input clock signal;

delaying the second input clock signal the first time period to produce a delayed second input clock signal; and

adding the remaining time period of the first input clock signal to the delayed second input clock signal.

5. The method of claim 4, wherein the static component is a static component of the clock signal time period.

6. The method of claim 4, wherein the static component is greater than the clock signal time period.

7. A method of synchronizing with a clock signal comprising:

receiving a clock signal having sequential first and second clock signal time periods;

delaying the first clock signal time period a first time delay;

delaying the first clock signal time period a second time delay equal to a real data path;

measuring a remaining component of the first clock signal time period upon receiving the second clock time signal period;

reproducing the remaining component of the first clock signal time period;

merging the reproduced remaining component of the clock signal time period to the second clock signal time period to produce a merged clock signal time period; and

delaying the merged clock signal time period the first time delay.

8. The method of claim 7, wherein the first time delay is a static component of the first clock signal time period.

9. The method of claim 7, wherein the first time delay is greater than the first clock signal time period.

10. An SMD circuit comprising:
a clock source;
a first delay segment coupled to the clock source;
a forward delay line coupled to the first delay segment;
an SMD control circuit coupled to the forward delay line and to the clock source; and
a backward delay line coupled to the clock source, the SMD control circuit, and coupled to a second delay segment.

11. The SMD circuit of claim 10, wherein the second delay segment has a time delay that is a fraction of a time period of the clock source.

12. The SMD circuit of claim 10, wherein the second delay segment has a time delay that is larger than a time period of the clock source.

13. The SMD circuit of claim 10, wherein the first delay segment has a time delay that is equal to the sum of the time delay of the second delay element and a data path model time period.

14. An integrated circuit comprising:
a clock input buffer coupled to receive a clock signal with a time period;
a first delay segment coupled to the clock input buffer;
a forward delay line coupled to the first delay segment;
an SMD control circuit coupled to the forward delay line and to the clock input buffer; and

a backward delay line coupled to the SMD control circuit, the clock input buffer, and to a second delay segment.

15. The integrated circuit of claim 14, wherein the second delay segment has a time delay that is a sub-part of the time period of the clock signal.

16. The integrated circuit of claim 14, wherein the second delay segment has a time delay that is greater than the time period of the clock signal.

17. The integrated circuit of claim 14, wherein the first delay segment has a time delay that is equal to the sum of the time delay of the second delay element and a data path model time period.

18. A memory device comprising:
an address interface;
a data interface;
a control interface; and
a SMD clock recovery and skew adjustment circuit comprising,
a clock input buffer coupled to receive a clock signal,
a first delay segment coupled to the clock input buffer,
a forward delay line coupled to the first delay segment,
an SMD control circuit coupled to the forward delay line and to the clock input buffer, and
a backward delay line coupled to the SMD control circuit, the clock input buffer, and to a second delay segment.

19. The memory device of claim 18, wherein the memory device comprises synchronous memory.

20. The memory device of claim 18, wherein the data interface further comprises a data latch coupled to the SMD clock recovery and skew adjustment circuit.

21. The memory device of claim 18, wherein the data interface further comprises a DQS strobe circuit coupled to the SMD clock recovery and skew adjustment circuit.

22. A DDR memory device interface circuit comprising:
a data interface;
a DQS signal interface;
a data latch coupled to the data interface; and
an SMD clock recovery and skew adjustment circuit coupled to the data latch and coupled to the DQS signal interface, wherein the SMD clock recovery and skew adjustment circuit comprises,
a clock input buffer coupled to receive a clock signal with a time period,
a first delay segment coupled to the clock input buffer,
a forward delay line coupled to the first delay segment,
an SMD control circuit coupled to the forward delay line and to the clock input buffer, and
a backward delay line coupled to the SMD control circuit, the clock input buffer, and to a second delay segment.

23. The DDR memory device interface circuit of claim 22, wherein the first delay segment has a time delay that is equal to the sum of the time delay of the second delay element and a data path model time period.

24. The DDR memory device interface circuit of claim 22, wherein the DDR memory device interface circuit is implemented in an ASIC.

25. The DDR memory device interface circuit of claim 22, wherein the DDR memory device interface circuit is implemented in a memory device.

26. A method of synchronizing with a clock source comprising:
coupling a first delay segment to a clock source;
coupling a forward delay line to the first delay segment;
coupling an SMD control circuit to the forward delay line and to the clock source; and
coupling a backward delay line to the SMD control circuit and to a second delay segment.

27. The method of claim 26, wherein coupling a backward delay line to the SMD control circuit and to a second delay segment further comprises coupling a backward delay line to the SMD control circuit and to a second delay segment, where the second delay segment has a time delay that is a portion of a time period of the clock source.

28. The method of claim 26, wherein coupling a backward delay line to the SMD control circuit and to a second delay segment further comprises coupling a backward delay line to the SMD control circuit and to a second delay segment, where the second delay segment has a time delay that is larger than a time period of the clock source.

29. The method of claim 26, wherein coupling a first delay segment to a clock source further comprises coupling a first delay segment to a clock source, where the first delay segment has a time delay that is equal to the sum of the time delay of the second delay element and a data path model time period.

30. The method of claim 26, further comprising selecting the first and second delay segments to match a non-variable portion of the time period of the clock source.

31. A method of synchronizing a memory device with a clock source comprising:
receiving a first clock signal on an interface of the memory device;
coupling the first clock signal from the interface through a first delay segment;
coupling the first clock signal from the first delay segment through a forward delay line;
measuring the progress of the first clock signal in the forward delay line with an SMD control circuit upon receiving a second clock signal on the interface;
inputting the second clock signal and an output of the SMD control circuit to a backward delay line; and
coupling the second clock signal from the backward delay line to a second delay segment.

32. The method of claim 31, wherein coupling the first clock signal from the interface through a first delay segment further comprises coupling the first clock signal from the interface through a first delay segment, where the first delay segment has a time delay that is equal to the sum of the time delay of the second delay element and a data path model time period.

33. The method of claim 31, wherein the memory device comprises non-volatile memory.

34. The method of claim 31, wherein the memory device comprises synchronous memory.

35. The memory device of claim 34, wherein the memory device comprises SDRAM memory.

36. The memory device of claim 34, wherein the memory device comprises DDR memory.

37. The method of claim 31, further comprising:
coupling the second clock signal from the second delay element to a data latch.

38. The method of claim 31, further comprising:
coupling the second clock signal from the second delay element to a DQS strobe circuit.

39. A method of synchronizing a memory device with a clock signal comprising:
receiving a first clock signal on an interface of the memory device;
coupling the first clock signal from the interface through a first delay segment;
coupling the first clock signal from the first delay segment through a data path model,
coupling the first clock signal from the data path model through a forward delay line;
measuring the progress of the first clock signal in the forward delay line with an SMD control circuit upon receiving a second clock signal on the interface;
coupling the second clock signal from the interface through a first delay segment; and
coupling the second clock signal from the first delay segment and an output of the SMD control circuit to a backward delay line.

40. The method of claim 39, wherein the memory device comprises non-volatile memory.

41. The method of claim 39, wherein the memory device comprises synchronous memory.

42. The memory device of claim 41, wherein the memory device comprises SDRAM memory.

43. The memory device of claim 41, wherein the memory device comprises DDR memory.

44. The method of claim 39, further comprising:
coupling the second clock signal from the backward delay line to a data latch.

45. The method of claim 39, further comprising:
coupling the second clock signal from the backward delay line to a DQS strobe circuit.